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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,158	06/27/2003	Nathan Laredo	TRAN-P206	7870

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EXAMINER	
TANG, KENNETH	

ART UNIT	PAPER NUMBER
2195	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/609,158	LAREDO ET AL.	
	Examiner	Art Unit	
	KENNETH TANG	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 are presented for examination.

2. This action is in response to the Remarks on 10/20/08. Applicant's arguments have been fully considered but they are considered moot in view of the new grounds of rejections.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-30 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, the following is indefinite:

- In line 9, it is unclear what element is "receiving an I/O access from the virtual machine application".
- In line 11, it is unclear in the claims where the "host operating system" is located.
- In line 12, it is unclear where the "state data" that is updated is located. It is unclear if it is in the VM application itself or elsewhere.
- In line 14, it is unclear what "resuming execution" is resuming from. No connection or relationship has been established.
- In the limitations of lines 9-14, there is no relationship or connection established with the instruction interpreter or the processor architecture and it is unclear in the claims of its association/relationship.

In claim 1, the following lacks antecedent basis:

- In line 9, "the virtual machine application" lacks antecedent basis.

4. Claims 11 and 21 are rejected for the same reasons as stated in the rejection of claim 1, and claims 2-10, 12-20, and 22-30 are also rejected as being dependent on rejected claims 1, 11, and 21.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Devine et al. (hereinafter Devine) (US 6,397,242 B1) in view of Dornan et al. (hereinafter Dornan) (US 7,089,539 B2).

6. Dornan was cited in Form 892 from the previous office action as relevant prior art but not used in that office action. Dornan is now applied as a new secondary reference in combination with Devine.

7. As to claim 1, Devine teaches a method for supporting input/output for a virtual machine (see Fig. 1-2), comprising:

executing virtual machine application instructions, wherein the application instructions are executed (col. 2, lines 27-35, col. 9, lines 11-12, etc.);

receiving an I/O access from the virtual machine application (col. 2, lines 21-36, col. 13, lines 20-36, Fig. 1-2);

upon receiving the I/O access, generate an exception (col. 7, lines 6-13, col. 8, lines 40-43);

performing the I/O access by using a host operating system (col. 11, lines 34-40, col. 12, line 50);

updating state data for the virtual machine application in accordance with the I/O access (col. 5, lines 60-67 through col. 6, lines 1-6); and

resuming execution of the virtual machine application (Resume 242, Fig. 2, col. 21, lines 56-60).

8. Devine is silent in the micro architecture code of a processor architecture code configured to feed pipelines of the processor architecture hardware, including an instruction interpreter to execute the virtual machine application instructions. However, Dornan discloses a computer system with micro architecture code of a processor code to feed pipelines of the processor architecture hardware, including a hardware instruction interpreter to execute the VM application instructions (Abstract, col. 1, lines 47-67, Fig. 11, item 126). Devine and Dornan are analogous art because they are both in the same field of endeavor of executing a virtual machine. One of ordinary skill in the art would have known to modify Devine's virtual machine system such that

it would include the processing hardware device for executing virtual machine instructions that include an instruction feeding means to the pipelines of the processor architecture hardware, as taught in Dornan. The suggestion/motivation for doing so would have been to provide the predicted result of being able to use the hardware interpreter to focus on performance critical mappings to produce a significant performance gain with relatively little additional hardware overhead (col. 2, lines 2-6, Abstract). Therefore, it would have been obvious to one of ordinary skill in the art to combine Devine and Dornan to obtain the invention of claim 1.

9. As to claim 2, Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches wherein the micro architecture code includes an instruction interpreter is further configured to function with an instruction translator to translate target instructions into host instructions to execute the virtual machine application instructions. Devine teaches that virtual machine processing with a VLIW architecture (col. 2, lines 30-36).

10. As to claim 3, Devine (Fig. 2, 230) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches wherein the micro architecture code includes an instruction translator to execute the virtual machine application instructions.

11. As to claim 4, Devine teaches further comprising: executing a monitor to implement the I/O access from the virtual machine application, wherein the monitor is configured to handle the exception caused by the I/O access (virtual machine monitor, see Abstract, col. 5, lines 13-30).

12. As to claim 5, Devine teaches further comprising:

entering the single step mode, wherein the monitor single steps through the application instructions to handle the exception (col. 11, lines 34-48, col. 12, lines 49-52).

13. As to claim 6, Devine (col. 24, lines 63-67) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teaches further comprising: using the monitor to maintain at least one virtual device to implement the I/O access from the virtual machine application.

14. As to claim 7, Devine teaches further comprising:

using the host operating system to access a real device in response to an access to the virtual device (Fig. 7, 700, 720, 750, 710, 100, col. 24, lines 60-67, etc.); and

updating the state data for the virtual machine application in accordance with I/O data retrieved from the real device (col. 5, lines 60-67 through col. 6, lines 1-6).

15. As to claim 8, Devine (see Fig. 1, col. 2, lines 27-35, col. 9, lines 11-12) and Dornan (Abstract, col. 1, lines 47-67, Fig. 11, item 126) teach wherein the virtual machine application instructions comprise target instructions and the micro architecture code comprises host instructions.

16. As to claim 9, Devine (col. 2, line 32) teaches wherein the target instructions are x86 instructions and the host instructions are VLIW instructions.

17. As to claim 10, Devine teaches wherein the virtual machine is an x86 compatible virtual machine (col. 9, lines 7-11).

18. As to claim 11, Devine teaches a system for supporting input/output for a virtual machine (Fig. 1-2), comprising:

a processor architecture including micro architecture code configured to execute, natively on a CPU hardware unit of the processor architecture (col. 2, lines 27-35, col. 9, lines 11-12); and

a memory coupled to the processor architecture, the memory storing virtual machine application instructions, wherein the application instructions are executed using the micro architecture code, the micro architecture code causing the processor architecture to implement a method comprising (col. 13, lines 20-36):

receiving an I/O access from the virtual machine application (col. 25, lines 14-21, etc.);

upon receiving the I/O access, generating an exception (col. 25, lines 14-21, etc.);

performing theI/O access by using a host operating system (Fig. 7, 700, 720, 750, 710, 100, etc.);

updating state data for the virtual machine application in accordance with the I/O access (col. 5, lines 60-67 through col. 6, lines 1-6); and

resuming execution of the virtual machine application (Resume 242, Fig. 2, col. 21, lines 56-60).

19. Devine is silent in the micro architecture code of a processor architecture code configured to feed pipelines of the processor architecture hardware, including an instruction interpreter to

execute the virtual machine application instructions. However, Dornan discloses a computer system with micro architecture code of a processor code to feed pipelines of the processor architecture hardware, including a hardware instruction interpreter to execute the VM application instructions (Abstract, col. 1, lines 47-67, Fig. 11, item 126). Devine and Dornan are analogous art because they are both in the same field of endeavor of executing a virtual machine. One of ordinary skill in the art would have known to modify Devine's virtual machine system such that it would include the processing hardware device for executing virtual machine instructions that include an instruction feeding means to the pipelines of the processor architecture hardware, as taught in Dornan. The suggestion/motivation for doing so would have been to provide the predicted result of being able to use the hardware interpreter to focus on performance critical mappings to produce a significant performance gain with relatively little additional hardware overhead (col. 2, lines 2-6, Abstract). Therefore, it would have been obvious to one of ordinary skill in the art to combine Devine and Dornan to obtain the invention of claim 11.

20. As to claims 12-21, they are rejected for the same reasons as stated in the rejections of claims 2-11.

21. As to claims 22-30, they are rejected for the same reasons as stated in the rejections of claims 2-10.

Response to Arguments

22. Applicant's arguments have been fully considered and found to be persuasive. However, new grounds of rejections based on Devine in view of Dornan render the arguments moot.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- **Masera et al. ("A quantitative approach to the design of an optimized hardware interpreter for Java byte-code", 1999)** teaches that a hardware implementation of an interpreter can overcome performance limits especially if dedicated hardware is provided. In this work a quantitative approach is developed to define a RISC superscalar micro-architecture offering an efficient execution of Java programs: accurate measurements of the most significant execution features led to anoptimized processor architecture (see Abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth Tang whose telephone number is (571) 272-3772. The examiner can normally be reached on 8:30AM - 6:00PM, Every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Meng-Ai An/
Supervisory Patent Examiner, Art Unit 2195

/Kenneth Tang/
Examiner, Art Unit 2195